IN THE SPECIFICATION

Please replace the paragraph at page 2, lines 18-31, with the following rewritten paragraph:

Figure 5 shows a second prior art that employs an extended source region 104, instead of the SAS structure. However, the extended source region 104 of Fig. 5 increases a cell size. Namely, a distance Ll shown in Fig. 6 must ~~sufficiently~~ be long enough to absorb positioning errors in a lithography process, prevent variations in the shapes of channel regions, and avoid unstableness in memory cell characteristics, in particular, between vertically formed memory cells. A distance L2 shown in Fig. 6 must also be ~~sufficiently~~ large enough to prevent a floating gate isolation region 128 from overlapping the source region 104 in the lithography process. If the overlapping happens, the source region 104 will be etched off in an etching process that follows the lithography process. It is difficult to maintain the shape of the ~~The~~ island-shaped floating gate isolation region 128 ~~is difficult to maintain is shape~~. If there are positioning errors between the floating gate isolation regions 128 and control gates 100 to vary the shapes of the control gates 100 between even and odd lines, there will be large cell characteristic differences between the even and odd lines.

Please replace the paragraph at page 5, lines 2-20, with the following rewritten paragraph:

Figure 7 shows a reference of the present invention that forms local wiring serving exclusively for source regions. In Fig. 7, stripe-shaped source regions 104 are connected to each other through high-melting point metal wiring 118 made of, typically, tungsten (W). To form the metal wiring 118, an additional manufacturing process is needed. In addition, the high-melting point metal wiring 118 requires a drain contact 120 to be extended through

interlayer insulating films 122 and 123, to connect a drain region 102 to metal wiring 124 serving as a bit line. This results in increasing an aspect ratio, insufficiently filling the contacts 120 with metal, and increasing the resistance of the contacts 120. The resistance drops further than connecting through the diffusion layer, when the source regions are connected to each other through the high-melting point metal wiring 118. But a wiring resistance of the high-melting point metal wiring 118 is higher than a wiring resistance of a metal wiring. There are ~~ease~~ cases in which many memory cells exist in the array and in which it connects a large number of source diffusion regions and the case in which the resistance value becomes a problem ~~far~~. The performance is lowered ~~lowers~~, when the resistance value is not low enough ~~low~~. It is necessary ~~that~~ for the resistance to be ~~is~~ reduced by connecting a source diffusion layer through metal wiring 45 for the source parallel placed with a bit line in ~~some~~ every some cells, as shown in Fig. 8, in order to prevent the lowering of the performance.